

42P17003

IN THE CLAIMS

Please amend the claims as follows:

1 (Currently amended). A reconfigurable chip including:

first and second multiplexers; and

a multiplication block including at least one a first multiplication unit and a group of selectable an adder unit units operably connected to the multiplication unit, wherein the adder units are selectively connectable in different configurations, a first configuration coupling first and second inputs of the first multiplication unit to outputs of the first and second multiplexers to receive first and second operands, and a second configuration coupling first and second inputs of the adder unit respectively to the outputs of the first and second multiplexers to receive the first and second operands;
and

multiple multiplier units and multiple adder units reconfigurable to provide an output that is a summed output of the multiplier units, a multiplier output or an adder output.

2 (Currently amended). The reconfigurable chip of claim 1 ~~wherein the multiplication block further comprises input multiplication multiplexers for the block wherein the first and second configurations are selected by an instruction supplied to the multiplication block.~~

3 (Currently amended). The reconfigurable chip of claim 2, ~~wherein there are fewer block input multiplexers than input multiplexers for the multiplication units further including a second multiplication unit having first and second inputs coupled to outputs of the first and second multiplexers.~~

4 (Currently amended). The reconfigurable chip of claim 1, ~~wherein the adder units include input multiplexers 3, further including a third configuration with the adder unit having first and second inputs respectively coupled to outputs of the first and second multiplication units.~~

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Claims 5-17 (Canceled).

18(Currently amended). A reconfigurable chip including:

a multiplication block including ~~at least one input multiplexer~~ first and second multiplexers, a multiplication unit having first and second inputs, and first and second operably connected to the input multiplexer, a group of ~~selectable~~ operably connected to the multiplication unit, wherein the ~~adder units are selectively connectable in different manners; and~~

wherein a first configuration instruction to an instruction memory storing multiple instructions for the multiplication block configures the multiplication unit to receive first and second operands from the first and second multiplexers and provide a product of the operands at an output, and a second configuration instruction configures the first and second adder units to receive the first and second operands from the first and second multiplexers and provide a summed value of the operands.

Claims 18-48 (Canceled).